HKN ECE 110 Review Session
Exam 3

COREY SNYDER

STEVEN KOLACZKOWSKI

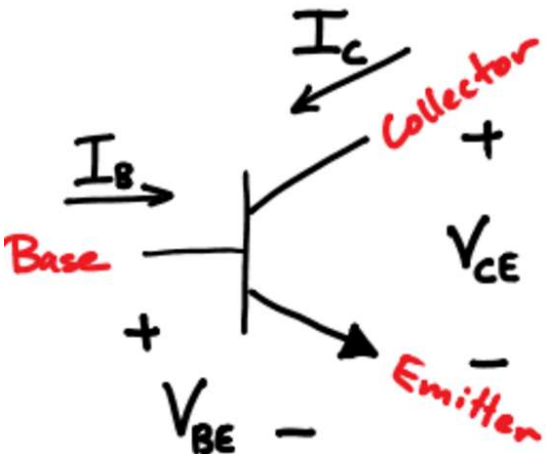
Reminders

- You are allowed one 8.5x11” note sheet (two-sided)
- Additional office hours help
- Course staff applications

Time	Monday	Tuesday	Wednesday	Thursday	Friday
9	All office hours are held in 1005 ECEB unless otherwise indicated. NAMES IN RED, EXAM WEEKS ONLY!				
10	PROF. GRUEV	NOMAAN	PROF. GRUEV	REWA	OSCAR, NOMAAN
11	MADDIE	MADDIE	PROF. SCHMITZ	NOMAAN	PROF. SCHMITZ, ARI
12					
1	ARI	SIMRAN	LIAN	LIAN	COREY, REWA
2	PROF. CHEN	NOMAAN	PROF. CHEN	STEVEN	COREY, SOPHIA
3	PROF. CHOI (2050 ECEB)		PROF. CHOI (2032 ECEB)*		HOMEWORK DUE!
4	STEVEN	ARI	NOMAAN	ARI	COREY, STEVEN
5	NAUMAN	ARI	OSCAR	GHAYOOR, REWA	COREY, STEVEN
6				GHAYOOR, REWA	
7	NAUMAN	GHAYOOR	GHAYOOR	COREY, REWA	
8	NAUMAN	GHAYOOR		COREY, REWA	
9	* 10/5: Room 2050				

Bipolar Junction Transistor (BJT)

- Three terminal device: Base, collector, emitter
- $V_{BE,ON}$ and $V_{CE,SAT}$ are properties of the BJT (ECE 340!)
- In ECE 110 we consider the Common-Emitter (CE) configuration
  - For more on this, take ECE 342!
- Three regions of operation: Off (Cutoff), Active, Saturation
- Off: $V_{BE} < V_{BE,ON}$, all currents are zero!
- Active: $V_{BE} > V_{BE,ON}$, $I_C = \beta I_B$
- Saturation: $V_{BE} > V_{BE,ON}$, $V_{CE} = V_{CE,SAT}$, $I_C \neq \beta I_B$!



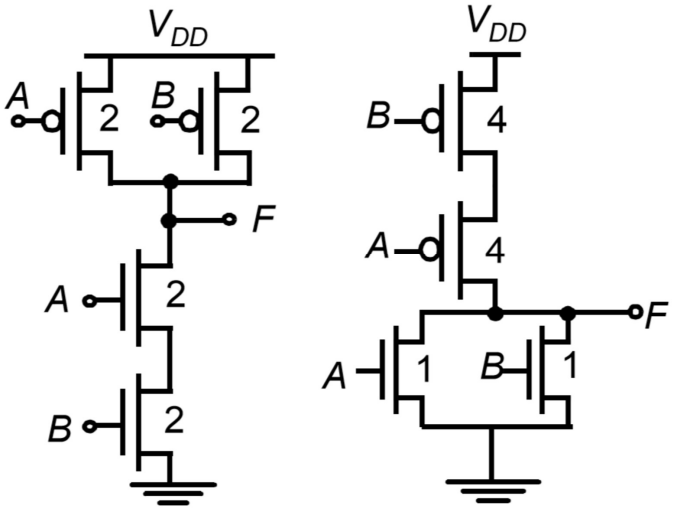
Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

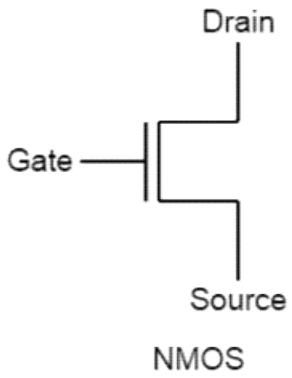
- Three terminal device: gate, source, drain
- Comes in two flavors, NMOS and PMOS, more on this in the next slide!
- V_{TH} is a property of the specific MOSFET (hello again ECE 340)
- Be comfortable interpreting I-V Characteristic of MOSFET

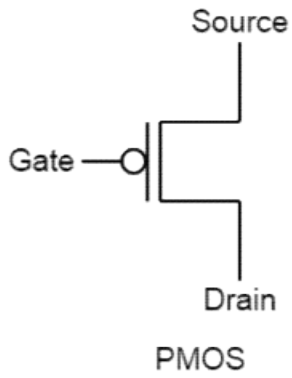
Conditions	Mode	Behavior under Linear Model
$V_{GS} < V_{TH}$	OFF	$I_D = 0$
$V_{GS} > V_{TH}$ $V_{DS} > V_{GS} - V_{TH}$	ACTIVE	$I_D = k(V_{GS} - V_{TH})^2$
$V_{GS} > V_{TH}$ $V_{DS} < V_{GS} - V_{TH}$	OHMIC	$I_D = k(V_{GS} - V_{TH})V_{DS}$

Complementary MOS Logic (cMOS)

- Combine NMOS and PMOS transistors in order to perform a logical operation
  - i.e. AND, NOR, NOT
- NMOS and PMOS are biased differently
  - NMOS, source connects to ground; PMOS, source connects to V_{DD}







Oh yeah and…

$$P = nafCV_{DD}^{2}$$

- n = number of capacitors
- a = activity factor
- f = frequency
- C = capacitance
- V_{DD} = applied voltage

Wise Words to Make your Score Soar

- Use your note sheet more like a study tool
- Spend your time showing what you know
- Make sure to get through the whole exam
- Look at past exams
- Take the time to relax before your exam